REMARKS

Claims 1-19 are pending. By this amendment, the specification and claims 4, 6, 11 and 13-18 are amended. No new matter has been added. Applicants respectfully request reconsideration and timely withdrawal of the pending objections and rejections for the reasons discussed below.

Allowed Claims

Applicants appreciate the indication that claims 17-19 contain allowable subject matter and would be allowed if presented in independent form. As claim 17 has been presented in independent form, Applicants respectfully request that at least claim 17 be indicated to be allowed. Claims 18 and 19 are not being presented in independent form at this time. Moreover, Applicants submit that all claims are in condition for allowance for the following reasons.

Specification

The Examiner requested that Applicants review the specification for errors. Applicants have reviewed the specification and, by the instant Amendment, are correcting some minor errors found therein.

Objection to the Claims

Claims 18 and 19 were objected to because they did not properly represent certain recited values in superscript. Applicants note that the originally filed claims 18 and 19 used the correct superscript values. Applicants, however, presented claims 18

and 19 in response to the Restriction Requirement with the incorrect superscript values even though the claims were identified as original claims.

Since claims 18 and 19 as presented in the instant Amendment did not change these values relative to the originally filed claims, Applicants are again presenting claims 18 and 19 in the instant Amendment as if these values have not been changed

Applicants respectfully request that the above-noted claim objection be withdrawn.

35 U.S.C. §102(b) Rejections

Claims 1, 5 and 7

Claims 1, 5 and 7 are rejected under 35 U.S.C. §102(b) as being anticipated by U.S. Patent No.: 6,277,720 to DOSHI, *et al.* ("DOSHI"). This rejection is respectfully traversed.

In order to establish a *prima facie* case of anticipation under 35 U.S.C. § 102, a single prior art reference must disclose each and every element as set forth in the subject claim. *Verdegaal Bros. v. Union Oil Co. of California*, 814 F.2d 628, 631, 2 USPQ 2d 1051, 1053 (Fed. Cir. 1987). Applicants respectfully submit that a *prima facie* case of anticipation cannot be established because DOSHI fails to teach each and every element of the claims.

Specifically, independent claim 1 recites, *inter alia,*

> depositing a nitride film along a surface of the substrate and the gate stack, wherein the nitride film is thicker over a surface of the substrate and thinner over a portion of the gate stack.

Applicants submit that DOSHI does not disclose, or even suggest, at least this feature. Applicants acknowledge, for example, that Fig. 2a shows a substrate 2, a gate structure 10 and a nitride layer 30. However, it is clear that this document does not specifically disclose or suggest the nitride film is thicker over a surface of the substrate and thinner over a portion of the gate stack.

Moreover, while the Examiner has alleged that DOSHI discloses this feature at col. 8, lines 8-22, it is clear from a fair reading of this language that DOSHI does not disclose or suggest that the nitride layer 30 can have different thicknesses, much less, that the nitride film is thicker over a surface of the substrate and thinner over a portion of the gate stack.

Applicants emphasize that col. 8, lines 8-22 of DOSHI merely states as follows:

> According to the preferred embodiment of the invention, silicon nitride layer 30 is now formed overall, preferably by way of low-pressure chemical vapor deposition (LPCVD), resulting in the structure illustrated in FIG. 3b. Nitride layer 30, as mentioned above and as described hereinbelow, will serve as a dopant barrier to boron and phosphorous residing in subsequently deposited doped silicon dioxide. It is preferred that nitride layer 30 be as thin as possible to minimize its etch time; however, nitride layer 30 must be sufficiently thick to have full integrity over the topography present in integrated circuit 20 to present a good barrier to dopant diffusion. In this embodiment of the invention, the thickness of nitride layer 30 may range from 65 Å to 250 Å; the illustration of nitride layer 30 in FIG. 3b and the succeeding Figures is therefore not necessarily to scale.

While it is true that such language discusses a desired thickness range of the nitride layer, the Examiner is not correct that this language discloses the nitride film is thicker over a surface of the substrate and thinner over a portion of the gate stack. In fact, Applicants submit that DOSHI only requires the nitride layer to be as thin as possible to minimize etch time, but thick enough to have full integrity over the transistor.

In contrast, in the invention, the nitride film may be absent (eliminated) completely on the gate stack sidewall (see paragraph [0031]), which would be contrary to DOSHI.

Thus, Applicants respectfully submit that independent claim 1 and dependent claims 5 and 7, which depend from claim 1 are allowable.

Accordingly, Applicants respectfully submit that the rejection under 35 U.S.C. § 102(b) should be withdrawn.

Claims 8-14

Claims 8-14 are rejected under 35 U.S.C. §102(b) as being anticipated by U.S. Patent No.: 6,153,501 to BECKER ("BECKER"). This rejection is respectfully traversed.

Specifically, independent claim 8 recites, *inter alia,*

> depositing a layer of nitride film over a gate stack and a surface of a substrate; and
> removing the nitride film on the gate stack to provide enhanced stress in a transistor channel under the gate stack.

Applicants submit that BECKER does not disclose, or even suggest, at least these features. Applicants acknowledge, for example, that Fig. 5 shows a wafer 50, a gate stack, and a nitride layer 62A disposed over these devices. Applicants also acknowledge that col. 3, lines 8-16 of BECKER appears to disclose that this layer can be removed at least partially from the gate stack using a resist layer 64. However, it is clear that this document does not specifically disclose or suggest that the nitride 62A is removed on the gate stack to provide enhanced stress in a transistor channel under the gate stack.

Moreover, while the Examiner has alleged that BECKER discloses this feature at col. 3, lines 8-16, it is clear from a fair reading of this language that BECKER does not

disclose or suggest removing the nitride film on the gate stack to provide enhanced stress in a transistor channel under the gate stack. This passage merely discloses that the spacer layer 62A is provided on the gate stack.

Applicants emphasize, for example, that col. 3, lines 8-16 of BECKER merely states as follows:

> As can be seen from FIG. 5, a spacer layer 62A such as oxide or nitride, or other layers, may be formed over layer 52A prior to the formation of the resist layer 64. As shown, this spacer layer 62 is formed over the front and back of the wafer, and over layer 52. If used, this layer is etched after its formation as shown in FIG. 5 using the resist layer 64 as a mask. Additionally, as shown in FIG. 6, other layers such as BPSG and TEOS can be formed over the front of the wafer subsequent to the etch step.

While it is true that such language discusses that the spacer layer 62A can be removed, the Examiner is not correct that this language discloses that the layer 62A is removed from the gate stack to provide enhanced stress in a transistor channel under the gate stack. BECKER is silent in this aspect of the invention.

Applicants also submit that the dependent claims are allowed on their own merits. For example, BECKER does not disclose or suggest forming the spacers along substantially all of the sidewall and etching the spacers to form spacers at the lower portion of the sidewalls (claim 13) or depositing at least one of an oxide layer or a borophosphorosilicate glass on low spots and leaving high spots exposed (claim 14).

Thus, Applicants respectfully submit that independent claim 8 and dependent claims 9-14, which depend from claim 8 are allowable.

Accordingly, Applicants respectfully submit that the rejection under 35 U.S.C. § 102(b) should be withdrawn.

35 U.S.C. § 103 Rejections

Claims 2-4 and 6 are rejected under 35 U.S.C. § 103(a) as being unpatentable over DOSHI in view of U.S. Patent No. 6,198,144 to PAN et al. ("PAN"). Claims 15 and 16 are rejected under 35 U.S.C. § 103(a) as being unpatentable over BECKER in view of PAN. These rejections are respectfully traversed.

In addition to the fact that DOSHI fails to disclose or suggest at least the features recited in claim 1 (from which claims 2-4 and 6 depend) and in addition to the fact that BECKER fails to disclose or suggest at least the features recited in claim 8 (from which claims 15 and 16 depend), Applicants submits that PAN also fails to disclose or suggest at least the features recited in at least claims 1 and 8.

Applicants acknowledge, for example, that the Abstract of PAN discloses that nitride spacers can be formed on sidewalls of a gate electrode stack. However, it is clear that this document, like that of DOSHI, is entirely silent with regard to depositing a nitride file on a substrate and the gate stack wherein the nitride film is thicker over a surface of the substrate and thinner over a portion of the gate stack. It is also clear that this document, like that of BECKER, is entirely silent with regard to depositing a layer of nitride film over a gate stack and a surface of a substrate and removing the nitride film on the gate stack to provide enhanced stress in a transistor channel under the gate stack.

Nor do any of the applied documents appear to disclose or suggest the enhancement of transistor performance by creating a desired stress in the transistor channel region as is the case with the instant invention.

Applicants note that DOSHI is merely concerned with using a nitride layer as a diffusion barrier (see Abstract) and is entirely unconcerned with creating a desired stress in the transistor channel region. Moreover, BECKER is entirely silent with regard to creating a desired stress in the transistor channel region. Finally, PAN is merely concerned with forming nitride spacers along sidewalls of the gate electrode stack to prevent conversion of conductive layers to non-conductive compounds during processing (see col. 2, lines 26-30) and is entirely silent and unconcerned with creating a desired stress in the transistor channel region. Thus, for at least the above-noted reasons, the asserted combinations of the above-noted documents are entirely improper.

Finally, Applicants also submit that the dependent claims are distinguishable over the applied documents. Consequently, allowance of claims 2-4, 6, 15 and 16 is respectfully requested.

Comments on Reasons for Allowance

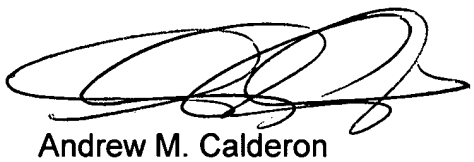
In response to the Statement of Reasons for Allowance set forth in the Office Action, Applicants wish to clarify the record with respect to the basis for the patentability of the indicated claims in the present application. In this regard, while Applicants do not disagree with the Examiner's indication that certain identified features are not disclosed by the references, Applicants submit that the claims in the present application recite a

combination of features, and that the basis for patentability of these claims is based on the totality of the recited features.

CONCLUSION

In view of the foregoing amendments and remarks, Applicants submit that all of the claims are patentably distinct from the prior art of record and are in condition for allowance. The Examiner is respectfully requested to pass the above application to issue. The Examiner is invited to contact the undersigned at the telephone number listed below, if needed. Applicants hereby make a written conditional petition for extension of time, if required. Please charge any deficiencies in fees and credit any overpayment of fees to **IBM Deposit Account No. 09-0458**.

Respectfully submitted,
Haining S. YANG, *et. al.*



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